PlatformConference

Direction • Design • Perspective • Analysis

Enabling High Performance IC Designs With HyperTransport IP Blocks

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Agenda

Need for speed

Why HyperTransport?

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About GDA Technologies

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Need for Speed

Our compute and networking customers are targeting higher speeds and bandwidths. The mood in those market segments can be summarized by the quote:

I feel the need; The need for speed!

Lt Pete "maverick" Mitchell (tom cruise) in top gun, 1986 action movie

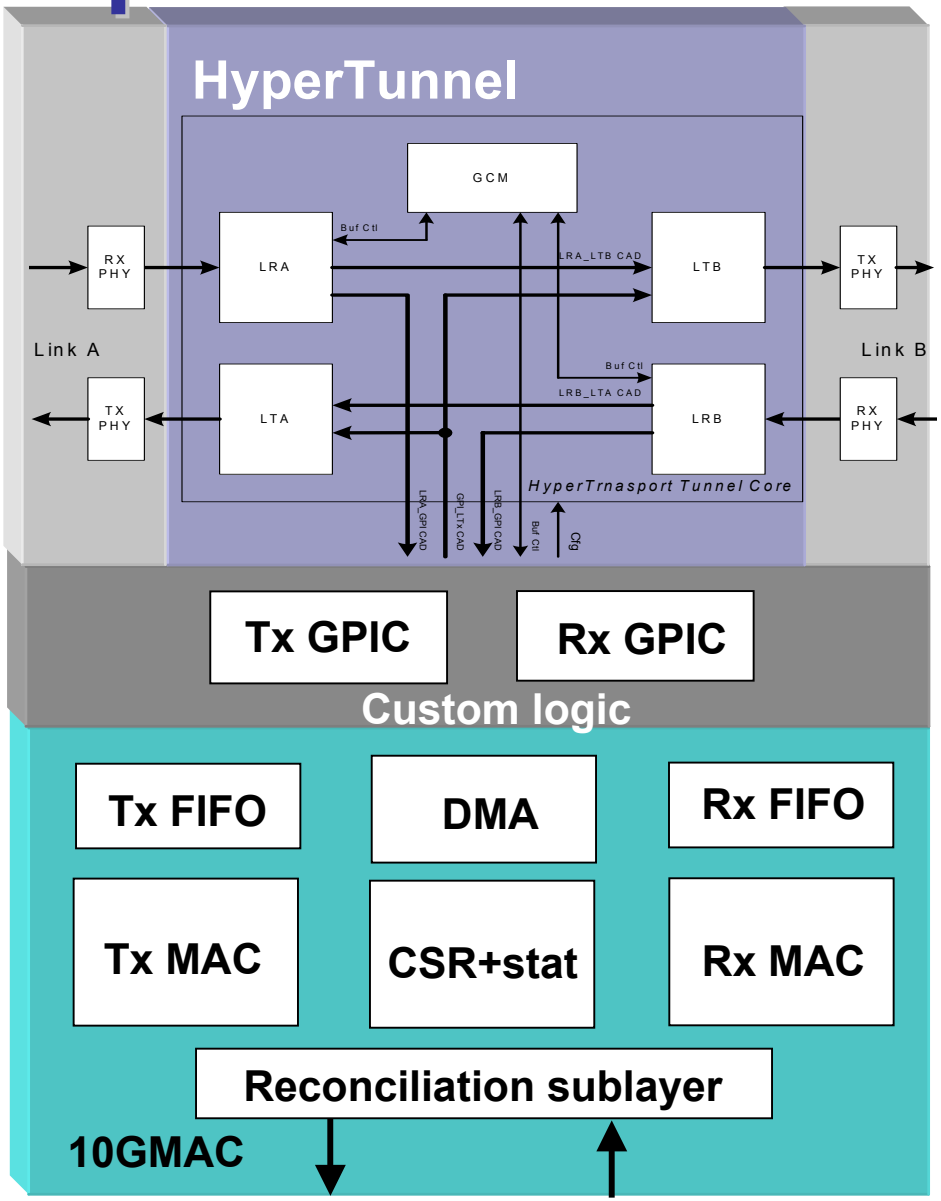
Why HyperTransport?

- New embedded system solutions demand very high IO bandwidth
- Today's high data rate networking solutions need multiple chips (port controllers, packet classifiers, protocol/security accelerators, processors etc.) And fast chip to chip interconnect
- PCI and derivatives fall short in bandwidth
- PCI and derivatives require too many pins
- High speed interfaces like SPI4 do not support addressing
- HyperTransport(HT) amply addresses the need. It is here. It is mature

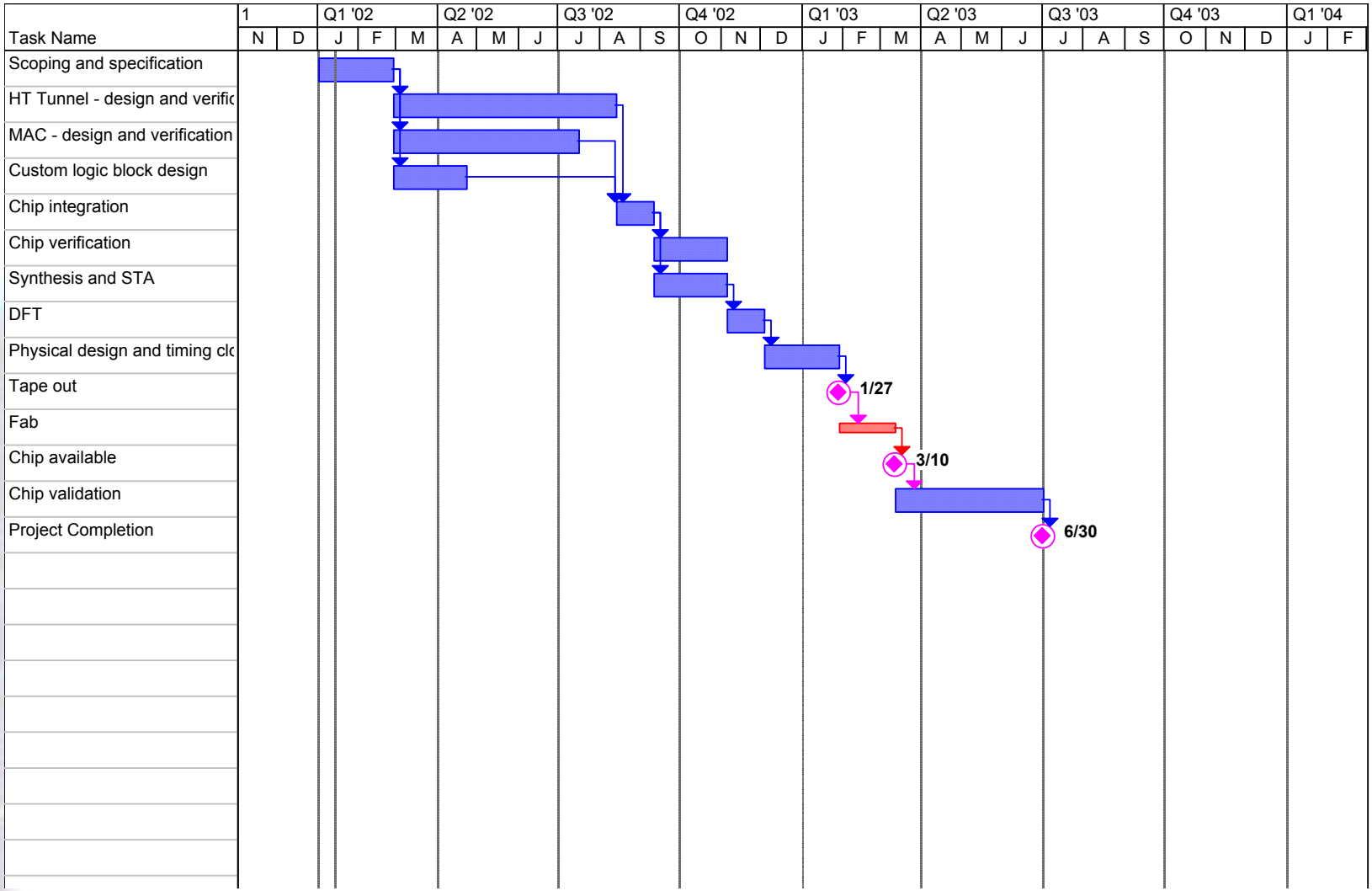
GDA's HyperTransport Program

- Tailored to enable fast time to market for HyperTransport based ICs
- Offers a fully compliant HyperTransport tunnel design – the common HT I/O building block
- Provides more than 200 test cases to cover the function and code exhaustively
- Provides the IP in netlist and hardmacro views
- Provides training and support on the IP deliverables
- Provides a suite of services to aid in different phases of development
- Partnership programs with PHY providers, FABs and tool vendors to provide complete solution

A development scenario - design



A development scenario - schedule



Areas of challenge

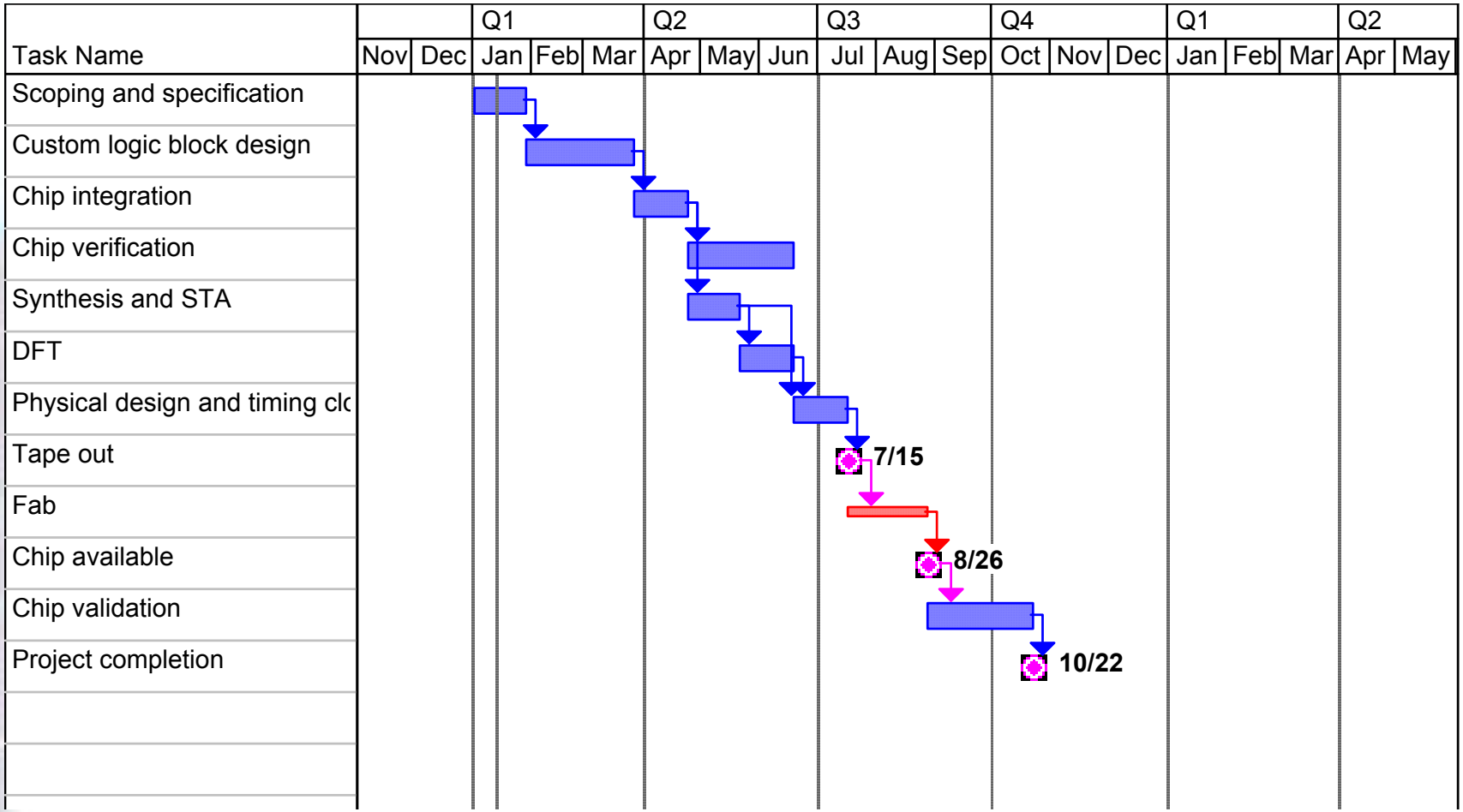
- Protocol compliance
- Timing issues in this ~100 Gbits/s (aggregate) design in 0.18u technology
- PHY selection
- PHY integration and timing
- Handling of HT interface on board design
- Chip validation and debug

GDA addresses these issues through the IPs, services and partnerships offered through its HyperTransport program.

Areas for optimization

- Block design for HyperTransport tunnel and 10G Ethernet MAC – GDA IP's eliminate these tasks
- Compliance verification of the tunnel and the MAC – GDA IP's eliminate these tasks
- Synthesis, STA and timing fixes – GDA IP's significantly simplifies this task
- DFT – IP core RTL and structure are DFT friendly
- Physical design – GDA's Hard macro licensing can drastically cut down this time
- Chip validation – Silicon proven IPs and GDA's expertise in validating those blocks shorten the effort

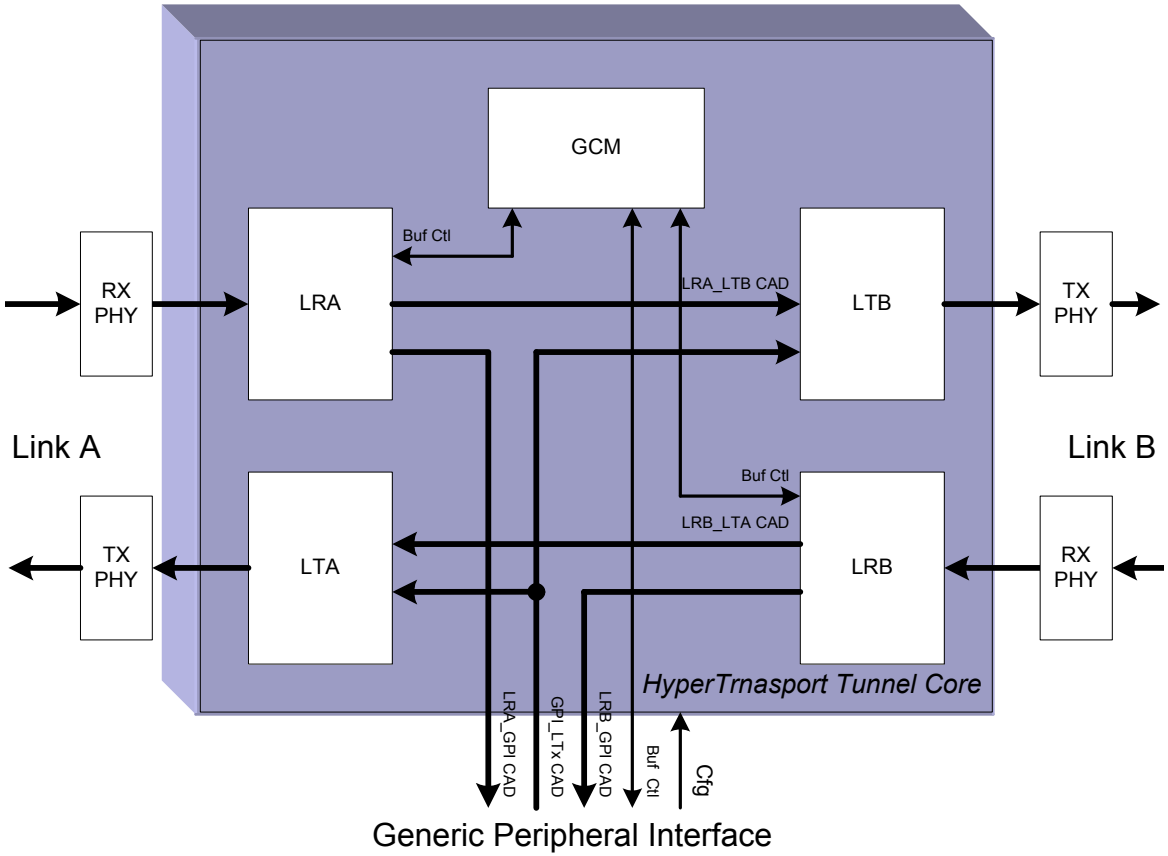
GDA Can Accelerate



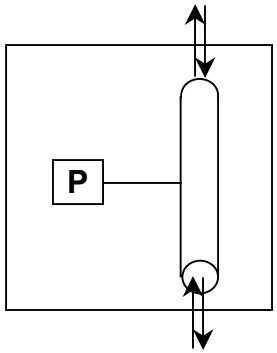
The changed development scenario

- GDA's HyperTransport program could
  - Reduce the development time by half
  - Reduce the development effort by 6 man years
  - Considerably reduce the risk by using proven IPs
  - Offer high confidence in overall solution through the partnerships with PHY providers and technology vendors

HyperTunnel Core



HyperTransport Tunnel



- HyperTransport tunnel is a dual-link device that acts as I/O channel building block. Tunnels allow creation of I/O channels through daisy-chaining.
- Packets received at one interface and not destined for the tunnel device itself are passed through to the second interface.
- More details on this topology can be found in the link specification.

HyperTunnel Features

- Compliant to HyperTransport IO Link Specification Version 1.03
- Dual HyperTransport links: link A and link B
- Port A is 16 bit wide. Supports link widths of 2/4/8/16 bits
- Port B is 8 bit wide. Supports link widths of 2/4/8 bits
- Maximum aggregate bandwidth of 6.4 GBytes/s in link A and 3.2 GBytes/s in link B
- A flexible back end interface for integration with user logic

HyperTunnel Features

- Either HyperTransport port can be configured as upstream
- Either port supports 200/400/500/600/800MHz
- Independent link width and frequency for each port
- Supports synchronous clocking mode
- Supports link disconnect protocol
- Supports external and internal loop backs on both HT ports
- 200 MHz, 128-bit internal data path
- Fully synchronous, technology-independent design

HyperTunnel deliverables

- RTL view of the tunnel design in Verilog
- Detailed design documentation
- Verification environment with drivers, checkers, bus monitors and protocol checkers
- Test cases for exhaustive code and functional coverage
- Synthesis environment for 0.18u technology

Standard service package

- Training on the design and deliverables
- Web based problem reporting and tracking for the support period
- FAQ and document updates made available through member's secure web account
- Telephone support during the support period
- Code updates and patches during the support period

Tools and formats

- HDL
  - Verilog
- Simulation
  - Cadence Verilog-XL
  - Cadence Verilog-NC
  - Synopsys VCS
- Synthesis
  - Synopsys Design Compiler
  - Cadence BuildGates (on request)
- Static Timing Analysis
  - Primetime

Target Applications

- Embedded processors, chip sets
- Routers, hubs, switches
- Set-top boxes
- Mobile/handheld devices
- Game consoles
- Any other application requiring high speed, low pin count, low latency and scalability

HyperTunnel Evaluation

- GDA offers a scheme to evaluate the HyperTunnel design through document review and simulation
- Sign up forms for the program can be found at http://hypertransport.gdatech.com
- The evaluation package includes:
  - User document for the core,
  - Encrypted RTL view
  - Encrypted test bench, and
  - Test cases
- For more details contact: ip@gdatech.com

Services Under HT Program

- IP customization
- Co-development of other HyperTransport IPs
- IP integration
- Netlist implementation for specific technologies
- Hard macro implementation for specific technologies
- Turn-key, HyperTransport-based IC design
- Board design and validation of HyperTransport systems
- Low level software development for HyperTransport systems
- Support for additional EDA tools (simulators, verification languages etc.)

About GDA Technologies, Inc.

- GDA Technologies is a 5 year old electronics design services (EDS) company with valuable IP portfolio, value added services, and high profile engineering resources
- GDA employs 175 engineers and has operations around the world: San Jose, Sacramento, Boston, Bangalore and Chennai
- Offers an IP portfolio of 20 high-value, reusable designs
- GDA provides ASIC/SOC, FPGA, board, embedded software and system design services
- GDA's focuses on designs in networking, computing and consumer electronics segments

IP Portfolio

Computing

- SDRAM controller
- Smart card
- AC-97
- PCI 32/33
- DMA controller
- USB dev 1.1
- I2S
- UART

Networking

- HDLC
- HyperTransport
- Utopia Level3
- POS-PHY Level3
- SPI-4 Phase2
- T1/E1
- 10G Ethernet MAC
- 1G Ethernet MAC

Signal processing

- Reed Solomon
- Viterbi
- FFT

More Information…

- Please check http://hypertransport.gdatech.com for more details and future updates on GDA's HyperTransport program
- Version 1.0 of HyperTunnel core is available NOW. Please contact ip@gdatech.com for licensing details
- A version update is planned for HyperTunnel core in the month of April, 2000 to offer more test coverage and some minor functional enhancements.